Successful Integration of Full Tram Priority in Greater Manchester's UTC Network:
Synchronising Controller Stage with UTC Plan Following Tram Priority Events

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ABSTRACT

Implementing tram priority operation at traffic signal sites which ordinarily operate in UTC, SCOOT or CLF mode, brings about unique challenges which would not normally be encountered on sites which operate in VA mode or under MOVA control.

UTC and CLF plans are unable to be influenced by external inputs and triggers; they represent the 'master' in the master-slave relationship which is present between UTC/CLF and the traffic signal controller stream. If the controller is released from UTC/CLF control by higher priority action, the controller is unable to provide feedback aimed at influencing the state of the UTC/CLF plan in order to keep the two synchronised. If the plan is not synchronised with the controller, demanded stages may be skipped leading to further disruption indirectly linked to the priority event.

For example, if a higher priority mode resulted in the current stage being held for longer than the UTC/CLF plan had intended, the plan itself would ideally also pause and only continue when the priority action was complete. This is of course how VA and MOVA operate, returning to normal operation without the added complexity associated with re-integration into a UTC/CLF plan.

This paper examines the complications associated with attempting to re-synchronise the controller's selected stage with the applied UTC or CLF force, and proposes a solution via the use of controller special conditioning.

INTRODUCTION

Greater Manchester is currently benefitting from a significant expansion of its Metrolink LRT network which includes a road traffic interface at around 80 new junctions.

There are many associated challenges from a traffic signal perspective; the junctions affected require the ability to deal with the following demands:

- Multiple stages may be necessary to service all traffic, pedestrian and tram phases.
- Co-ordination with adjacent signals via SCOOT/UTC/CLF may be required (alternatively, MOVA can be utilised and can be very beneficial as it is able to deal efficiently with priority events).
- Full tram signal priority with the goal of reducing tram delays to zero wherever possible.

The complications that the above bring to normal operation can best be described by first dividing the Light Rail Vehicle (LRV) priority event into distinct periods:

0. **Default Mode:** Junction is operating in the default mode (which would normally be SCOOT/UTC/CLF/VA/MOVA).
1. **LRV Prepare:** In order to ensure that the tram receives a 'proceed' signal before it arrives at the stop-line, the controller may prevent stage changes or select a different stage to overcome any stage change restrictions (disabling UTC/CLF in the process or requesting priority action in MOVA). In this period, non-cyclic stage changes may occur causing demanded stages to be skipped.
2. **LRV Priority Phase:** Tram transits through the junction ideally without needing to brake on approach.
3. **Skipped Stage Rectification:** Any skips that may have occurred should be addressed before attempting to return to the default mode (e.g. if a 2-5 move has occurred and stage 3 was not demanded but 4 was, a move to stage 4 would be the optimum choice). This can be achieved in a 'constrained' VA mode where certain stages are prevented.
4. **UTC (or CLF) Synchronisation:** Controller returns to normal operation. If returning to UTC/CLF mode, this will potentially create new 'stage skipping' problems as the controller's selected stage is unlikely to agree with the requested UTC/CLF force; as a result, demand dependent windows may be missed. To remedy this problem, the controller should attempt to synchronise its selected stage with the applied UTC/CLF force in a regulated way without causing further disruption.

Periods 1 and 2 (which are associated with the preparation of the junction and the servicing of the priority phase) are well established basic requirements at sites with tram priority. Periods 3 and 4 are often given less attention (if any), but become more important as junction saturation levels, intersection complexity (number or competing stages) and priority vehicle frequency increase. Period 3 can be catered for correctly using the following methodology which is usually reserved for sites with greater than 4 stages:

- 'Skip' flags are set for any demanded stage which is skipped on a move to the priority stage.
- If any skip flags are set, moves to stages which do not have skip flags set are prevented. This ensures that all skipped stages are serviced in cyclic order under VA logic before the controller returns to the default mode.
- Demand dependency is also considered at UTC/CLF sites such that skip flags are not set if a demand dependent window passed unused as the stage demand was not present when the window was open.

It is the Period 4 logic on which this paper is focused. Experiments using controller configuration files currently held for existing sites in Tameside and Salford have indicated that the conditioning required to facilitate the UTC (or CLF) synchronisation facility is possible and can produce very favourable results; it is intended to trial the facility at the Trafford Road / Ordsall Lane signals in Salford during September 2013. The modified configurations have been tested extensively on the Siemens IC4 emulator package and demonstrate that skipped stages can be entirely eliminated during the recovery period using this new facility.

Synchronising Controller Stage with UTC/CLF Plans

Priority action occurring in Periods 1 and 2 may cause the controller's selected stage to be either advanced or delayed relative to the UTC/SCOOT/CLF plan running in the background. The purpose then of Period 4 is to reverse the effect that the priority action had on the controller cycle time by either expanding or compressing the stage lengths in order to synchronise with UTC/CLF (and without skipping stages).
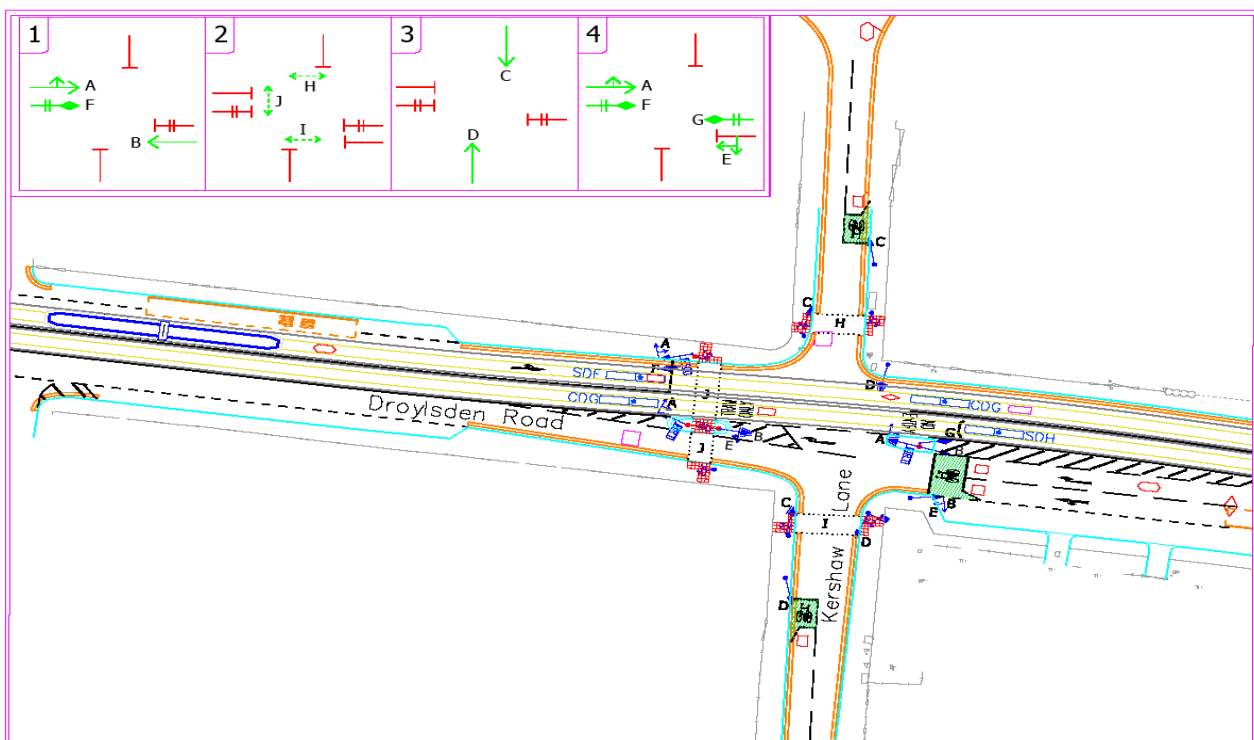

Figure 1: Droylsden Rd / Kershaw Lane plan

Fig. 1 shows the Droylsden Road / Kershaw Lane signal plan. This junction is used to show how the UTC or CLF synchronisation action can be applied to a 4 stage site.

UTC and CLF can be considered to be very similar in the way they influence the controller stage. UTC plans can be written to mimic CLF plans and vice versa. There are a few subtle differences, but in essence, the mechanisms described in this paper can be considered to apply equally to both UTC and CLF scenarios; as such, only UTC will be discussed in detail.

Difficulties Associated with Mode Switching Priority Events

The following diagram shows how the controller selected stage and subsequent G-bit confirmation follows the UTC force influence in a typical plan (with all stages demanded and extended). This scenario shows the controller in 'Period 0', i.e. the controller is operating in default mode (on a UTC plan) without the complications associated with a tram priority event.
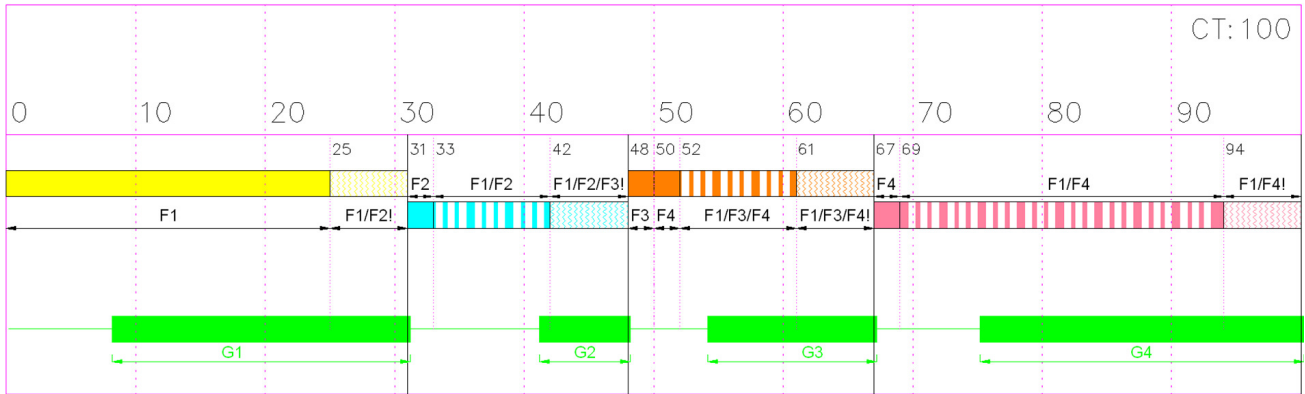

Figure 2: Typical UTC plan with corresponding controller response

Taking the Kershaw Lane junction as an example, 3 of the 4 stages are demand dependent and as such only receive a short window (normally 1 or 2 seconds) in which a stage change can occur if the preceding stage was demanded and extended to its maximum. Stages 2, 3 and 4 are demand dependent; the windows for these stages are represented in Fig. 2 by blocks of solid colour (these are periods where only the F-bit corresponding to the demand dependent stage is present).

As the window periods are relatively short, it is important that the controller is suitably prepared to perform a stage change when the window opens, i.e. the controller must be *in* stage with no controlling phase minima active. If the controller is unable to perform a stage change by the time the window closes, the opportunity to move to the demand dependent stage will pass and the stage will be skipped in normal UTC operation. This scenario is very likely to occur when the controller is taken to a higher priority mode of operation to service a tram demand for example, and then returns to the default UTC mode (especially if the priority event had caused the stage lengths to be increased or an additional stage had been serviced).
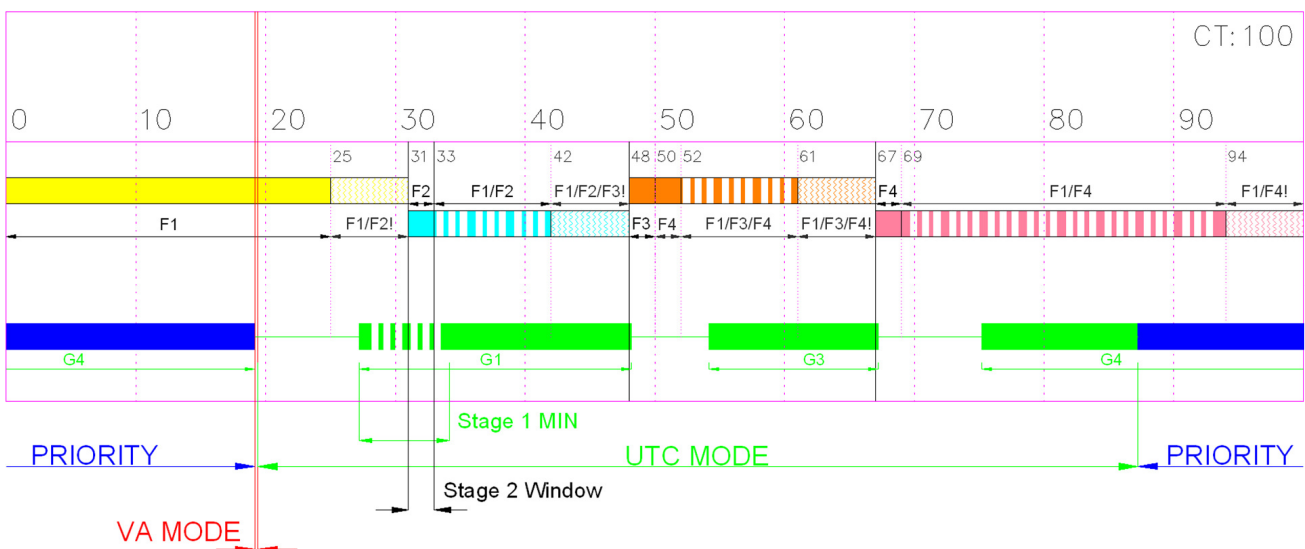

Figure 3: Typical UTC plan interrupted by a priority event with resultant controller response

Fig. 3 shows how disruptive a priority event can be to the stage sequence. In the example shown, a priority event is initiated at approximately 87 seconds (with reference to the 100 second cycle time). Assuming that the priority event is a relatively uncomplicated affair and that the controller is requested to merely hold stage 4 until the priority phase is serviced, the net result can still be problematic operationally. After the priority phase is serviced, the controller will normally revert to VA mode to perfom a stage change to the next demanded stage before attempting to return to the default mode.

Fig. 3 shows that stage 4 has been held in priority mode well into the period in which stage 1 is forced. When the stage change to 1 finally occurs, the controller is unable to run stage 1 to the end of its minimum green before the stage 2 window expires. As a result, **stage 2 is skipped** and the applied combination of UTC forces (F1/F2) ensures that stage 1 is held until the stage 3 window opens.

Returning to UTC: Plan / Stage Synchronisation

After the controller has dealt with any skips which may have occurred as a result of the preparatory action associated with the priority event, the controller will then return to UTC. Complexities will arise if the controller stage is significantly 'out of phase' (not synchronised) with the UTC plan.

As previously described, priority events can be considered to compress, expand or have a neutral effect on the controller cycle time when referenced against the UTC plan. When the controller attempts to return to UTC, it can perform the following operations to either compress or stretch the stage lengths until the controller's selected stage agrees with the applied UTC force.

- **Stage length compression:** Select VA mode and mask phase extensions (alternatively, 'Hurry Call' mode could be utilised).
- **Stage length expansion:** Prevent stage changes in VA mode (or use 'prohibited/ignored stage moves' facility to prevent backwards moves).

In order to make an accurate assessment of the 'phase shift' that may be present between the controller stage and the UTC plan, the controller must be able to monitor the current UTC force even when UTC mode is disabled during a priority event.

To prevent compliance faults being logged at the UTC in-station, the controller would normally set the Hurry Call reply bit (HRY) for the entire duration of the tram priority event. The purpose of this is to inform the in-station that the controller will be unable to comply with the UTC plan; in turn, the in-station then stops sending force bits until the HRY bit is reset.

Rather than setting the HRY bit for the entire duration as described above, it is preferable to set HRY for only a nominal period of approximately 6 seconds at the start of Period 1 (at the commencement of the LRV Prepare action). The force bits then return shortly after the HRY bit is dropped allowing the controller to start to monitor the status of the incoming UTC force bits (even though the priority event is well and truly underway). The UTC in-station will tolerate non-compliance with the applied UTC forces for a configurable time following the removal of the HRY bit (normally around 2 minutes). So, as long as the priority period and subsequent UTC recovery is completed by the time the UTC in-station compliance checks are restarted, the UTC system will not report a fault that the stage green confirm bit (G-bit) is not agreeing with the force bit (F bit).

The UTC recovery facility is achieved entirely in controller conditioning at present. The action required needs careful consideration as to whether stage compression or expansion is necessary. It is helpful to show this graphically in matrix form.

	UTC/CLF 1		UTC/CLF 2			UTC/CLF 3				UTC/CLF 4		
	F1	F1/F2!	F2	F1/F2	F1/F2/F3!	F3	F4 (FALSE)	F1/F3/F4	F1/F3/F4!	F4	F1/F4	F4/F1!
	CLF FORCE 1	PREVENT EXCEPT 2	CLF FORCE 2	HOLD	PREVENT EXCEPT 3	CLF FORCE 3	CLF FORCE 4	HOLD	PREVENT EXCEPT 4	CLF FORCE 4	HOLD	PREVENT EXCEPT 1
STAGE 1				ADVANCE	ADVANCE	ADVANCE	ADVANCE	ADVANCE	ADVANCE	HOLD		
STAGE 2	ADVANCE						ADVANCE	ADVANCE	ADVANCE	ADVANCE	ADVANCE	ADVANCE
STAGE 3	ADVANCE	ADVANCE	HOLD	HOLD							ADVANCE	ADVANCE
STAGE 4		ADVANCE	ADVANCE	ADVANCE	ADVANCE	HOLD						

Figure 4: Recovery action **decision** matrix

Fig. 4 (the recovery action *decision* matrix) shows what action the controller should take if the selected stage is not in agreement with the UTC/CLF force. The applied UTC/CLF force is shown along the top row, whilst the controller stage is shown in the left hand column. Any action decided upon is only enacted when the controller is free to perform a stage change, i.e. the controller is in stage and there are no active controlling phase minima. The cells which contain no colour indicate that the UTC/CLF plan *is* in agreement with the controller stage and that synchronisation is not necessary (or the synchronisation process is complete).

If the controller stage is equal to the requested stage + 1 for example, it would follow that cycle time expanding action is necessary in order for the UTC/CLF plan to 'catch up' with the controller. Conversely, if the controller stage is equal to the requested stage −1 or −2, then cycle time compression is required with the resultant action being to 'ADVANCE' to the next stage as quickly as possible.

It may however, not always be appropriate to hold a stage if the stage in question is a pedestrian stage or filter stage for example. In these cases, deferring the 'HOLD' action until the controller is in the next stage may be necessary.

	UTC/CLF 1		UTC/CLF 2			UTC/CLF 3				UTC/CLF 4		
	F1	F1/F2!	F2	F1/F2	F1/F2/F3!	F3	F4 (FALSE)	F1/F3/F4	F1/F3/F4!	F4	F1/F4	F4/F1!
	CLF FORCE 1	PREVENT EXCEPT 2	CLF FORCE 2	HOLD	PREVENT EXCEPT 3	CLF FORCE 3	CLF FORCE 4	HOLD	PREVENT EXCEPT 4	CLF FORCE 4	HOLD	PREVENT EXCEPT 1
STAGE 1				GO TO VA & MASK EXTS if... Stage 2 Demanded*		GO TO VA & MASK EXTS if... Stage 2 Demanded*	GO TO VA & MASK EXTS if... Stage 2 Demanded* OR, Stage 3 Demanded*			IGNORED MOVE		
STAGE 2	GO TO VA if... Stage 3 Demanded* OR, Stage 4 Demanded*						GO TO VA if... Stage 3 Demanded*			GO TO VA if... Stage 3 Demanded*	GOT TO VA if... Stage 3 Demanded* OR, Stage 4 Demanded*	
STAGE 3	GO TO VA & MASK EXTS if... Stage 4 Demanded*		PREVENT 3-2 MOVE IN UTC/CLF MODE								GO TO VA & MASK EXTS if... Stage 4 Demanded*	
STAGE 4		GO TO VA & MASK EXTS	GO TO VA & MASK EXTS			IGNORED MOVE						

*Stage demands only valid if the stage was demanded when the associated UTC/CLF window was open

Figure 5: Recovery action **mechanism** matrix

Fig. 5 (the recovery action *mechanism* matrix) shows how the decisions described in Fig. 4 would be realised by the controller. Where cycle time compression is required (indicated in Fig. 4 by 'ADVANCE'), the following events would occur:

- Controller disables UTC/CLF mode which produces a mode change to the fall-back, VA.
- Controller masks phase extensions.
- A stage change to the next demanded stage occurs in VA mode.
- Controller returns to UTC/CLF mode.

When cycle time expansion is required (as described in Fig.4 by 'HOLD'), the mechanism is somewhat simpler, and is achieved as follows:

- Either, the controller stays in UTC/CLF mode and 'Prohibited/Ignored Moves' are configured which prevent a stage change (as the move is not allowed); or
- Stage changes are prevented in controller conditioning.

Dealing with Demand Dependency

Controller action to compress the cycle time will only occur if the controller has first ascertained that the stages which would otherwise be skipped by an immediate return to UTC *were* demanded when their respective windows were open. For example, if following a priority event the controller is in stage 2 and the UTC/CLF requested stage is 4, a move to stage 3 will only be required if stage 3 was demanded when the window for stage 3 was open. This is standard logic in UTC mode in that a stage change to a demand dependent stage will not occur if the demand did not exist when the window was open. So, if the stage 3 demand was only received after the window closed, the controller would remain in UTC/CLF mode and a change to stage 4 would ensue as per standard UTC logic.

Fig. 6 below shows how the proposed remedial controller action serves to synchronise the selected stage with the UTC plan when a priority event has caused the cycle time to expand (stage 4 has been extended).
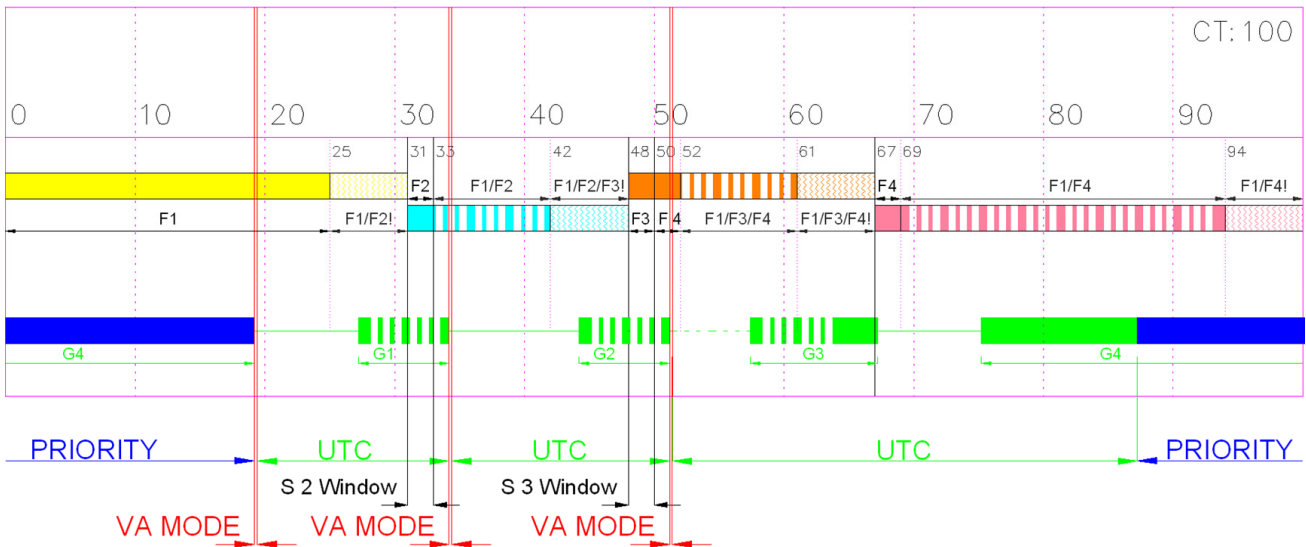

Figure 6: Typical UTC plan and controller response to a priority event incorporating synchronisation strategy

The scenario displayed above shows a priority event that occurs at the same time, and has the same duration as the scenario described in Fig. 3 (the priority event starts at 87 s and the tram is clear of the junction after the controller performs a VA change to stage 1 at 19 s). In the unmodified scenario described in Fig. 3, the controller skips stage 2 because stage 1's minimum green is active during the stage 2 window. Fig. 6 shows how the controller attempts to synchronise itself with UTC at every opportunity necessary until synchronisation is complete.

Cycle time compression is required in Fig. 6; a VA change from stage 1 to 2 occurs as soon as the stage 1 minimum green has expired. As the stage 2 minimum green is then active whilst the stage 3 window is open, additional remedial action is also required in order that stage 3 is then serviced. Once again, as soon as the stage 2 minimum expires, an immediate VA change to stage 3 occurs.

As the UTC force for stage 3 is significantly longer than the minimum time required to run stage 3, the controller is able to complete the synchronisation process during stage 3. The definition of 'complete' can be considered to be the point at which the G-bit agrees with the F-bit and the stage minimum green is not active.

In order to achieve synchronisation as quickly as possible, the UTC plan must be sufficiently compressible, i.e. some of the stages must be forced for longer than their minimum durations. This will of course normally be the case; the scenario described only runs stage 2 for its minimum, with stages 1 and 4 having plenty of additional time allocated.

CONCLUSION

The UTC synchronisation facility described in this report may appear to be a relatively complex remedy to an issue which currently does not receive much attention from signal engineers. However, it *does* become a useful tool when maximum priority is required especially at more complex traffic signal controlled intersections.

When viewing a junction's operation from the perspective of the pedestrian, motorist or cyclist, the concept of either compressing or expanding the controller cycle time in response to a priority event can be considered an intuitive remedial reaction, especially when compared with the alternative unregulated (and apparently random) stage changes which would otherwise ensue.

It has been shown that stage skips can occur 2 stage changes after the priority event finishes. In fact, there are situations in which stage skips may occur even later. If the 2 stages which immediately follow the priority event are not demand dependent in UTC/CLF mode and are normally only forced for a minimum time, the third stage (if demand dependent), could be skipped as it is the first stage to have a short window. This is a situation which would appear to be entirely counter intuitive to the road-user who would be expecting to receive a green signal when it was 'their turn' in the signal sequence. Whereas the junction user may have tolerated a non-cyclic stage change event as a tram was on approach, a stage skip occurring significantly after the priority event was completed will probably cause frustration and may lead to driver non-compliance if the stage had also been delayed whilst the tram was approaching the junction.

It should be noted that the facility described has been developed in order to achieve the goal of absolute tram priority without producing significant disruption to the general traffic flows. There are

other priority control strategies available that serve to balance the needs of all junction users, effectively biasing (to some degree) the servicing of the priority vehicle stage over the other competing stages. Rather than granting absolute priority to the tram, these alternative options may sacrifice some level of priority in order to balance reducing delays to the tram against ensuring that the other competing stages are not seriously perturbed.

If the highest level of priority is required whilst maintaining co-ordination with other traffic signals via UTC/SCOOT/CLF, then the mechanisms described in this report can certainly assist in realising this goal especially at sites with multiple stages or relatively high degrees of saturation.

APPENDICES

The following text shows how the UTC synchronisation facility is produced for the demand dependent stage 2 referenced in the Kershaw Lane example. Similar blocks of conditioning are required for the 3 other stages; additional conditioning is also required in order to alter the appearance of the HRY bit for example.

```
IFT (F2.(NOT(F1+F3+F4)))+(CLFFRCST2.1SCRT238) THN        ; IF THE UTC/CLF STAGE 2 WINDOW IS OPEN...

IFT NOT(CNDTMA46+1SCRT202) THN
FALSE::=.1SCRT201                              ; ...SET FORCE 2 REFERENCE FLAG AND RESET FORCE
      *=.1SCRT203                              ; 1/3/4 FLAGS IF THE UTC/CLF WINDOW INHIBIT TIMER
      *=.1SCRT204                              ; IS NOT ACTIVE AND THE FORCE 2 FLAG IS NOT SET.
TRUE=+1SCRT202
RUN <46>                                       ; ...RESET THE UTC/CLF WINDOW INHIBIT TIMER
END

1SCRT202.DR2.NOT(NXTSTG0 EQL <2>)=1SCRT162     ; ...SET UNUSED WINDOW FLAG IF STAGE 2 NOT DEMANDED

ELS                                            ; IF THE STAGE 2 WINDOW IS NOT OPEN...

1SCRT202.1SCRT241.(NOT 1SCRT162):=+1SCRT240    ; ...DISABLE UTC/CLF & MASK EXTS IF FORCE 2 REF FLAG SET
                             *=+1SCRT239       ; IN STAGE 1 AND THE STAGE 2 UNUSED WINDOW FLAG NOT SET
END

1SCRT202.1SCRT244:=+1SCRT240                   ; DISABLE UTC/CLF AND MASK EXTS IF FORCE 2 REF FLAG SET
            *=+1SCRT239                        ; IN STAGE 4
```

1SCRT238 = Flag enabling CLF forces to be considered. Approximately 3 s after the HRY bit is reset, the in-station will recommence sending F bits. Rather than check the status of the CLF influence immediately, CLF is ignored until it can be assumed that UTC mode is not required.

1SCRT20X = 'Force Reference' flag. Describes the current UTC/CLF force X, which starts and ends when a new window opens (when a single F bit is present or a CLF Force exists).

1SCRT16X = 'Unused Stage X Window' flag. Set if a demand dependent window is open and there is no associated demand.

1SCRT24X = 'Stage X Free to Move' flag. Indicates that the current stage is able to move and there are no active controlling phase minima.

CNDTMA46 = Timer which prevents 'False Forces' being considered by the controller. Fig. 4 shows such a force (for stage 4), inserted after the UTC stage 3 window; its purpose is to provide an alternative stage change option should the preceding demand dependent window not be used. As the timer is started every time a new valid window opens, False Force windows are discounted as they will normally be inserted immediately after genuine demand dependant windows when the 'UTC/CLF window inhibit timer' will be active.